REMARKS

Claim 3 is amended to correct a typographical error.

Drawings

Applicant submits herewith a sketch showing proposed changes to Figs. 2 and 3 with changes shown in red in accordance with MPEP 608.02(v). Applicant requests the Examiner's approval of the proposed drawing changes in accordance with 37 CFR 1.121(a)(3)(ii) and MPEP 608.02(q).

Specification

The specification is amended to correct informalities as requested by the Examiner.

The Examiner has objected to the specification because a summary of the invention was not included. However, 37 CFR 1.73 states: "A brief summary of the invention ... *should* precede the detailed description. Such summary should, *when set forth*, be commensurate with the invention as claimed...." (*Emphasis added.*) The use of "should" and "when set forth" indicates that the summary is optional and not required.

Claim Rejections - 35 USC § 102

Claims 2-5, 10, 13, 19 and 22-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Underwood (U.S.P. 4,131,254). Applicant traverses this rejection.

Claim 2 recites that the differencing circuit is arranged to continuously process outputs from the first and second log amps. Underwood only discloses a circuit in which the outputs from two log amps are stretched by a sample and hold circuit. (Col. 3, lines 55-59.) Therefore, the rejection of claim 2 is overcome.

Claim 4, which is rewritten in independent form, recites that the differencing circuit is a summing node. The Examiner alleges that the differencing circuit inherently has a summing node. However, in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art. MPEP 2112. Underwood only discloses a summing amplifier (col. 3, line 67). The Examiner has not provided any basis as to why an amplifier would inherently be a node. Thus, the rejection of claim 4 is improper.

Claim 10, which is rewritten in independent form, recites that the first and second log amps are co-integrated on a substrate. The Examiner points to a statement made in Underwood that the log amps may be of integrated circuit construction, such as are obtainable from Texas Instruments and others. From this, the Examiner concludes that Underwood discloses two log amps that are co-integrated on a substrate. There is, however, no support for this conclusion. Nothing in Underwood teaches the co-integration of two log amps on a substrate. Moreover, the Examiner has not shown that two co-integrated log amps were available from any vendor or taught by any reference. Therefore, claim 10 is not anticipated by Underwood.

Claim 13 recites a parasitic network coupled to the first log amp. The Examiner alleges that item 26 of Underwood is a parasitic network. However, item 26 of Underwood is identified as a linear summing amplifier (col. 3, line 35) which would be implausible to describe as a parasitic network. Moreover, claim 13 depends from claim 12, which the Examiner essentially admits is not subject to rejection under 35 U.S.C. 102. Therefore, claim 13 could not possibly be anticipated by Underwood.

Claim 19 recites an integrated circuit comprising two or more log amps. The Examiner alleges that Underwood discloses such an apparatus at col. 3, lines 48-54. This part of Underwood, however, can only reasonably be read as disclosing two log amps fabricated as separate integrated circuits.

Claim 22 is amended to recite that the first and second output signals are processed differentially *and continuously*. Support for this limitation can be found in the specification at, for example, page 4, line 14. In contrast, Underwood only discloses a system in which the outputs from the log amps are in the form of pulses that are stretched by sample and hold circuits. (Col. 3, lines 55-59.) Thus, claim 22 is not anticipated by Underwood.

Claim 24, which is rewritten in independent form, recites that the first and second output signals are limiting output signals. Claim 24 also recites multiplying the first and second output signals. Underwood does not disclose first and second limiting output signals, nor does it disclose multiplying such signals. Therefore, claim 24 is not anticipated by Underwood.

Claim 25, which is rewritten in independent form, recites utilizing a signal to be examined as the first input signal, and utilizing a reference signal as the second input signal. Underwood does not disclose the use of a reference signal. The only signals disclosed by Underwood are signals A, B, C and D from a quadrant detector 12, all of which are examined to provide the sought after guidance signal (col. 3, lines 14-19). Claim 26 recites that the

reference signal has the same waveform as the signal to be examined. As discussed above, Underwood does not disclose *any* reference signal, much less one having the same waveform as the signal to be examined. Claim 27, which is rewritten in independent form, recites the utilization of modulated and modulation signals for the first and second inputs signals. Underwood does not disclose that any input signals that are logarithmically amplified are modulation or modulated signals. Thus, claims 25-27 are not anticipated by Underwood.

Claim Rejections - 35 USC § 103

Claims 6-7, 9, 16 and 18 are rejected under 35 U.S.C. 103(a) over Underwood (U.S.P. 4,131,254) in view of Fujii et al. (U.S.P. 5,731,698). Applicant traverses this rejection. A *prima facie* case of obviousness has not been established for any of these claims.

Claim 6, which is rewritten in independent form, recites a phase detector core coupled to the first and second log amps. The Examiner alleges that it would have been obvious to modify Underwood's system to include a phase detector core as disclosed by Fujii, but has not identified any valid suggestion or motivation to modify Underwood. The Examiner's stated reason for adding a phase detector to Underwood is that it would provide instantaneous detection of phase due to the use of the log amps. However, there is no support for this argument in either reference. Underwood does not disclose, or even suggest, the desirability of using a phase detector; thus, Underwood does not provide the motivation for combining the references. Fujii discloses a phase differencing circuit as prior art (col. 1, line 45), and also discloses the desirability of using instantaneously responding circuitry to drive the phase differencing circuit (col. 2, lines 12-34). Fujii then goes on to describe roughly 20 different embodiments of circuitry to provide instantaneous drive, but not a single one of these embodiments discloses or even suggests a logarithmic amplifier. Since neither of the references provides the required suggestion or motivation to combine the references, a *prima facie* case of obviousness has not been established.

Claim 7 recites that the log amps have limiting outputs. The Examiner argues that this is inherently disclosed in the prior art by the voltage source applied to the log amps. Although the output ranges of most analog circuits are eventually limited by the voltage source, the term "limiting", as used in the present application, is understood to refer to a mode of operation that intentionally produces a signal that is more like a square wave. (See, e.g., page 5, lines 11-14.) Underwood does not disclose or suggest this type of limiting output from a log amp, and therefore, cannot serve as a basis for an obviousness rejection.

Claim 16 recites first and second log amps having limiting outputs. The examiner alleges that Underwood discloses log amps having limiting outputs, but there is no support for this allegation in the reference. Nothing in Underwood suggests that the outputs from the log amps are anything other than simple analog outputs. Therefore, the obviousness rejection cannot be based on Underwood. Moreover, the Examiner's stated reason for combining the references--providing instantaneous response--is incorrect as discussed above with respect to claim 6.

Claim 18 recites that the first and second log amps are co-integrated on a substrate. As discussed above with respect to claim 10, there is, however, no support for this conclusion. Nothing in Underwood teaches the co-integration of two log amps on a substrate.

Claims 8 and 17 are rejected under 35 U.S.C. 35(a) over Underwood in view of Fuji and further in view of Lopez et al. (U.S.P. 5,530,349). Applicant traverses this rejection. This rejection is based on the same incorrect assumptions that underlie the rejection of claims 7 and 16, and therefore, there is no basis for the further application of Lopez.

Claim 11 is rejected under 35 U.S.C. 103(a) over Underwood in view of Ausschnitt (U.S.P. 4,538,105). Applicant traverses this rejection.

Claim 11 recites that the first and second log amps are arranged symmetrically about a center line. The Examiner alleges that Ausschnitt discloses first and second log amps arranged symmetrically about a center line. However, Ausschnitt does not disclose any log amps, much less log amps arranged around a center line. The Examiner points to a passage in Ausschnitt that discusses the desirability of positioning slots between conductive lines on a first level of an integrated circuit symmetrically with respect to the centerline of a pattern of conductive lines on a second level of the integrated circuit. Thus, Ausschnitt relates to conductive line spacing and does not disclose or suggest the desirability of arranging entire co-integrated log amps symmetrically about a centerline.

"One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988), quoting *W.L. Gore v. Garlock,* 220 USPQ 303, 312-13 (Fed. Cir. 1983). Here, the Applicant's disclosure has been used as a roadmap to pick and choose among isolated disclosures that provide no suggestion or motivation to combine the references. The only relevance of the Ausschnitt reference is that the word "centerline" is

found somewhere in the disclosure. The argument that it would have been obvious to combine the references for the purpose of improving the test wafer or integrated circuit is a *non sequitur*. Presumably, the purpose of *any* reference is to provide an improved or beneficial result. Thus, a *prima facie* case of obviousness has not been established.

Claim 14, 15 and 20 are rejected under 35 U.S.C. 103(a) over Underwood in view of Bradbury et al. (U.S.P. 5,534,854). Applicant traverses this rejection.

Claim 14, which is rewritten in independent form, recites a third log amp. Claim 15, which is also rewritten in independent form, recites one or more log amps in addition to the first and second log amps. Claim 20 recites (in its base claim) an integrated circuit comprising two or more log amps. The Examiner alleges that Underwood discloses two or more log amps in an integrated circuit. As discussed above, Underwood does not more than two log amps and does not disclose two co-integrated log amps. Therefore, Underwood cannot form a basis for this rejection. Moreover, the passage in Bradbury cited by the Examiner relates to comparators, not differencing circuits as recited in the rejected claims. Thus, a *prima facie* case of obviousness has not been established.

Claim 21 is rejected under 35 U.S.C. 103(a) over Underwood in view of Feeney et al. (U.S.P. 5,508,610). Applicant traverses this rejection.

Claim 21 recites (in its base claim) an integrated circuit comprising two or more log amps. The Examiner alleges that Underwood discloses two or more log amps in an integrated circuit. As discussed above, Underwood does not more than two log amps and does not disclose two co-integrated log amps. Therefore, Underwood cannot form a basis for this rejection. Regarding the Feeney reference, once again, Applicant's disclosure has been used as a roadmap to pick and choose among isolated disclosures. The only relevance of Feeney is that it happens to include a phase detector, but it provides no motivation or suggestion to combine the references. Therefore, a *prima facie* case of obviousness has not been established.

New Claims

New claims 28 and 29 are added. Support for these claims can be found in the specification at page 3, lines 24-26 and at page 4, line 15, respectively.

CONCLUSION

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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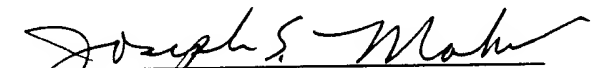

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please replace the paragraph beginning on page 3, line 3 with the following:

Log amp 10 will be referred to as part of channel A, which receives the input signal V_A and generates the logarithmic output signal V_{OUT_A}. Likewise, log amp 12 will be referred to as part of channel B, which receives the input signal $V[B]_B$ and generates the logarithmic output signal V_{OUT_B}. For purposes of illustration, the signals utilized in Fig. 4 are shown as single-sided voltages, but the present invention can be realized with differential voltage signals, differential or single-sided current mode signals, or any convenient combination thereof. The logarithmic output signals $V_{OUT}[A]_A$ and V_{OUT_B} are given by the following equations:

In the Claims:

Claim 1 is cancelled.

2. (Amended) A measurement system [according to claim 1 further comprising] comprising:

a first log amp;

a second log amp; and

a differencing circuit coupled to the first and second log amps, wherein the differencing circuit is arranged to continuously process outputs from the first and second log amps. (F)

3. (Amended) A measurement system according to claim 2 wherein:

the first log amp has a first logarithmic output coupled to a first input to the differencing circuit; and

the second log amp has a second logarithmic output coupled to a second input to the differencing circuit.

4. (Amended) A measurement system [according to claim 3] comprising:

a first log amp;

a second log amp; and

a differencing circuit coupled to the first and second log amps, wherein the differencing circuit comprises a summing node.

6. (Amended) A measurement system [according to claim 2 further comprising] comprising:

a first log amp;

a second log amp;

a differencing circuit coupled to the first and second log amps; and

a phase detector core coupled to the first and second log amps.

10. (Amended) A measurement system [according to claim 1] comprising:

a first log amp; and

a second log amp;

wherein the first and second log amps are co-integrated on a substrate.

14. (Amended) A measurement system [according to claim 2 further comprising] comprising:

a first log amp;

a second log amp;

a differencing circuit coupled to the first and second log amps; and

a third log amp coupled to the differencing circuit.

15. (Amended) A measurement system [according to claim 2 further comprising] comprising:

a first log amp;

a second log amp;

a differencing circuit coupled to the first and second log amps; and

one or more additional log amps coupled to the differencing circuit.

22. (Amended) A method comprising:

logarithmically amplifying a first input signal, thereby generating a first output signal;

logarithmically amplifying a second input signal, thereby generating a second output signal; and

differentially and continuously processing the first and second output signals.

24. (Amended) A method [according to claim 22] comprising:

logarithmically amplifying a first input signal, thereby generating a first output signal;

logarithmically amplifying a second input signal, thereby generating a second output signal; and

differentially processing the first and second output signals

wherein:

the first and second output signals are limiting output signals; and

differentially processing the first and second output signals comprises multiplying the first and second output signals.

25. (Amended) A method [according to claim 22 further comprising:] comprising:

logarithmically amplifying a first input signal, thereby generating a first output signal;

logarithmically amplifying a second input signal, thereby generating a second output signal;

differentially processing the first and second output signals;

utilizing a signal to be examined as the first input signal; and

utilizing a reference signal as the second input signal.

27. (Amended) A method [according to claim 22 further comprising:]

comprising:

logarithmically amplifying a first input signal, thereby generating a first output signal;

logarithmically amplifying a second input signal, thereby generating a second output signal;

differentially processing the first and second output signals;

utilizing a modulated signal for the first input signal; and

utilizing a modulation signal for the second input signal.

Claims 28 and 29 are new.